CLAIMS

What is Claimed is:

1. A method for providing read-only data to a requester, said method comprising:

receiving a plurality of address bits from said requester;

generating a plurality of binary values using two of said plurality of address bits and a plurality of logic functions; and

providing said read-only data to said requester, said read-only data including at least one of said plurality of binary values.

2. The method of Claim 1, wherein said receiving step further comprises receiving exactly two address bits from said requester.

3. The method of Claim 1 , wherein said generating step further comprises selecting said plurality of logic function from a list of logic functions consisting of AND, OR, XOR, NOT, NAND, NOR, and XNOR.

4. The method of Claim 2, wherein said generating step further comprises selecting said plurality of logic function from a list of logic functions consisting of AND, OR, XOR, NOT, NAND, NOR, and XNOR.

5. The method of Claim 1, wherein said providing step further comprises multiplexing said plurality of binary values to produce said read-only data.

6. The method of Claim 5, wherein said multiplexing step further comprises selecting at least one of said plurality of binary values based upon at least one of said plurality of address bits, said at least one of said plurality of address bits being separate and distinct from said two of said plurality of address bits.

7. A method for providing read-only data to a requester, said method comprising:

receiving a plurality of address bits from said requester;

generating a plurality of binary values using two of said plurality of address bits and a plurality of logic functions;

multiplexing said plurality of binary values to produce read-only data, said read-only data being based upon at least one of said plurality of address bits, said at least one of said plurality of address bits being separate and distinct from said two of said plurality of address bits; and

providing said read-only data to said requester.

8. The method of Claim 7, wherein said generating step further comprises generating said plurality of binary values by performing logical AND, OR, XOR, NOT, NAND, NOR, and XNOR operations on said at least two address data-bits and the negation of said at least two address bits.

9. The method of Claim 7, wherein said generating step further comprises selecting said plurality of logic functions from a list of logic functions consisting of AND, OR, XOR, NOT, NAND, NOR, and XNOR.

10. A read-only memory system where read-only data is stored in combinatorial logic, said system comprising:

at least one binary logic function device adapted to receive two binary address bits and to generate a plurality of binary values from said two address bits and a plurality of logic functions, said read-only data including at least one of said plurality of binary values

11. The read-only memory system of Claim 10, further comprising at least one multiplexer adapted to receive at least one of said plurality of binary values, said read-only data being provided from an output of at least one of said at least one multiplexer.

12. The read-only memory system of Claim 11, wherein said at least one multiplexer is adapted to select a subset of said at least one of said plurality of binary values based upon at least one address bit, said at least one address bit being separate and distinct from said two address bits.

13. The read-only memory system of Claim 10, wherein said plurality of logic functions are selected from a list of logic functions consisting of AND, OR, XOR, NOT, NAND, NOR, and XNOR.

14. The read-only memory system of Claim 11, wherein said plurality of logic functions are selected from a list of logic functions consisting of AND, OR, XOR, NOT, NAND, NOR, and XNOR.

15. The read-only memory system of Claim 12, wherein said plurality of logic functions are selected from a list of logic functions consisting of AND, OR, XOR, NOT, NAND, NOR, and XNOR.

16. The read-only memory system of Claim 12, wherein at least one of said at least one multiplexer is selected from a list of multiplexers consisting of 2:1, 4:1, 8:1, and 16:1 multiplexers.

17. The read-only memory system of Claim 11, further comprising at least one decoder for decoding said at least one address bit.

18. The read-only memory system of Claim 12, further comprising at least one decoder for decoding said at least one address bit.

19. The read-only memory system of Claim 18, further comprising at least one stage two multiplexer, where the output of said at least one multiplexer is provided to said at least one stage two multiplexer, the output of said at least one stage two multiplexer being said read-only data.

20. The read-only memory system of Claim 17, further comprising at least one stage two multiplexer, where the output of said at least one multiplexer is provided to said at least one stage two multiplexer, the output of said at least one stage two multiplexer being said read-only data.

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